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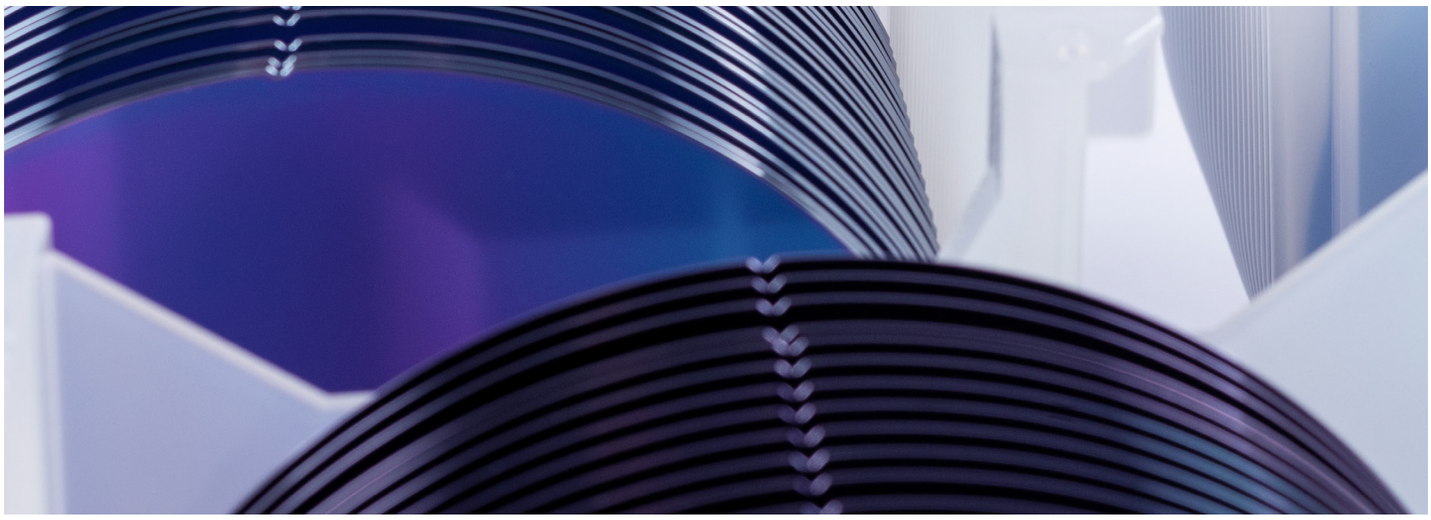


SILICON WAFERS OPTIMIZED FOR POWER DEVICE NEEDS

Power Management SOI Wafers

Bonded SOI wafers with down to <0.001 Ohm-cm resistivity, tight resistivity control, low and controlled Oi levels and low defect density. Gate drivers for power devices, Battery and Power Management ICs, Intelligent Power Modules, and other Smart Power devices using advanced BCD or BiCMOS processes. Also available as Terrace Free version.

Power GaN Substrate Wafers (Si)

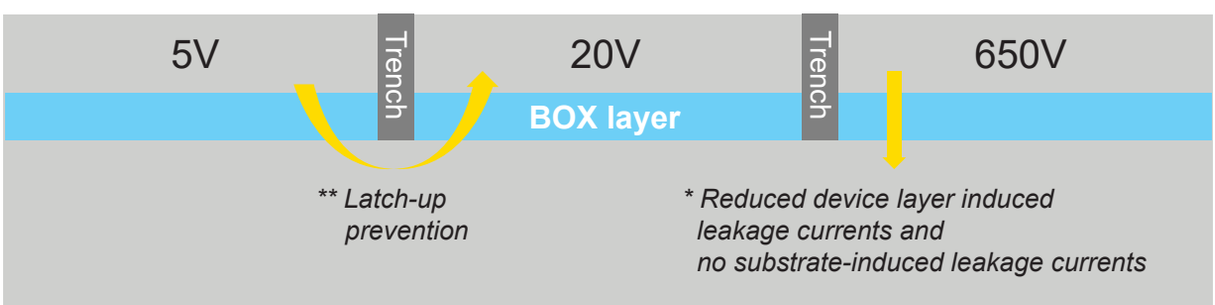
From standard to extra thick <111> Si and SOI wafers with advanced stress management for GaN growth. Customized for GaN-on-Si and GaN-on-SOI power device needs. Highly functional and cost-effective challenger for GaN-on-SiC substrates. Suitable for GaN HEMT devices.

Discrete Power Device Wafers

Discrete Power Device wafers offering customizable resistivity between <0.001 and >350 Ohm-cm, tight resistivity control, low and controlled Oi level and low defect density. Suitable for all discrete power devices (IGBTs and Power MOSFETs with low on-resistance).

Power Management SOI Enables Higher Voltages and Improved Isolation

- SOI BOX layer and trench isolation enables monolithic integration of low, medium and high voltage blocks on the same chip while reducing the chip size.
- Reduced leakage currents* compared to bulk Silicon wafers → improved performance during high frequency or high temperature operation.
- Latch-up prevention** and improved ESD/ EMI protection.
- Increases options to design driver high common-mode transient immunity (CMTI) without expensive galvanic/optical isolation.



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