OKMETIC

MORE DESIGN FREEDOM WITH BONDED SOI WAFERS

BSOI

Fully customizable with thick or thin device layer. Suitable e.g. for traditional MEMS devices. Also advanced options such as two device and BOX layers of diferent thicknesses. Also available as Terrace Free version.

E-SOI®

Highly uniform wafers with ±0.1 µm thickness variation. Suitable e.g. for silicon photonics and high-precision silicon-based MEMS. Also available as Terrace Free version.

C-SOI®

Wafers with embedded / buried cavities. Suitable e.g. for pressure and inertial sensors, silicon speakers, ultrasonic transducers, resonators and microfluidic devices.

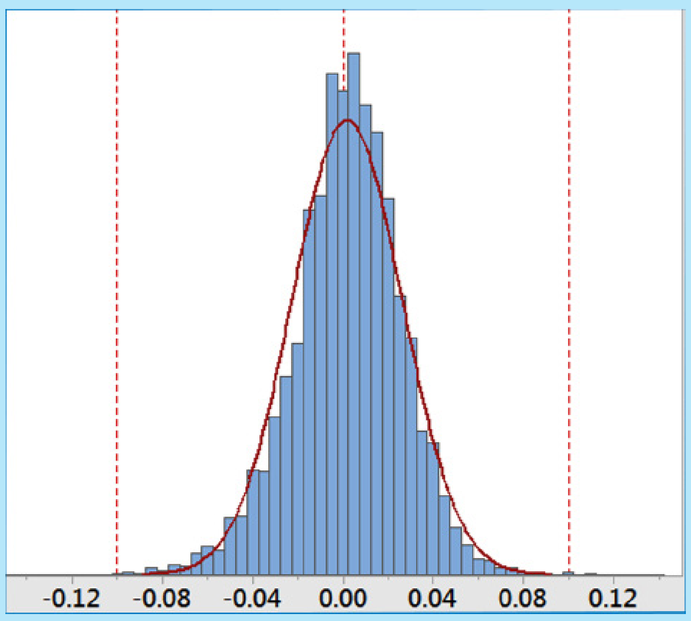
TSV – Through Silicon Vias

Polysilicon filled TSVs enable isolated electrical connections to be made through silicon wafers.

DESIGN FREEDOM, PERFORMANCE AND EASE OF MANUFACTURING

- Bonded SOI wafers provide an optimal platform for the manufacture of demanding MEMS, sensor, RF and power devices.
- Device manufacturers benefit from increased design freedom, maximum device performance, cost-effectiveness and ease of manufacturing.
- Customized wafer solutions to meet your device and process needs.
- SOI wafer volume production for leading semiconductor device manufacturers since 2001.
- Fully in-house process covering crystal growth, wafering, SOI bonding, DRIE and lithography.

Device layer thickness capability of E-SOI® wafers



Deviation from target thickness (µm)

TYPICAL SOI WAFER SPECIFICATIONS

RESISTIVITY

From <0.001 to >7,000 Ohm-cm

DEVICE LAYER THICKNESS

From 1 µm to > 200 µm

Tolerance ±0.5 µm (standard BSOI), ±0.1 µm (200 mm E-SOI®), ±0.5 µm (C-SOI®)

HANDLE WAFER THICKNESS

From 300 µm to 950 µm, typically 725 µm in 200 mm wafer and 380 µm in 150 mm

Back surface polished or etched

BURIED OXIDE

Type: thermal oxide, thickness: from 300 nm to 4 µm, typically between 0.5 µm and 2 µm