OKMETIC

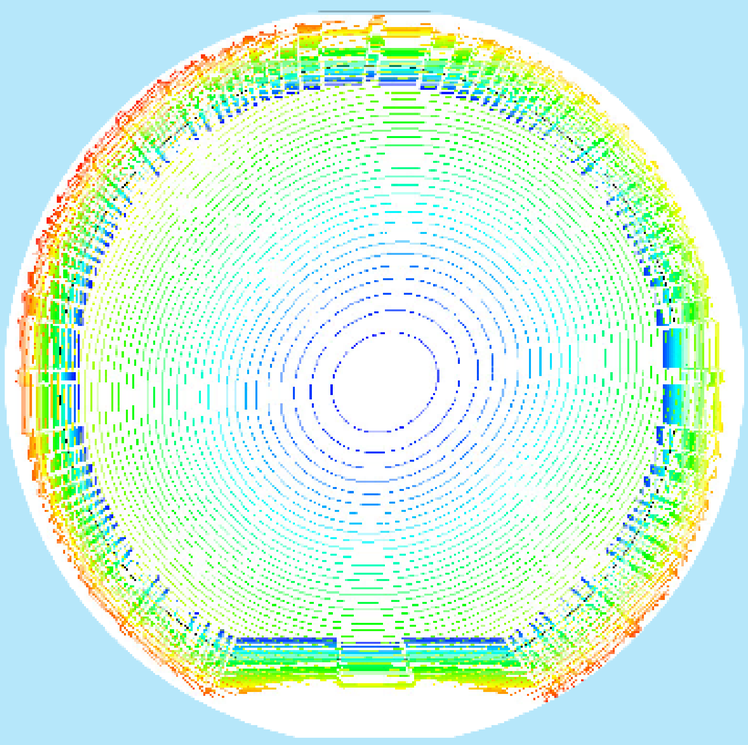
SILICON WAFERS OPTIMIZED TO ENDURE STRESSES OF GAN-ON-SI EPITAXY

SILICON WAFERS SOLUTIONS FOR POWER AND RF GAN-ON-SI APPLICATION NEEDS

- Silicon wafers that are designed to facilitate the growing of high-quality gallium nitride and to offset the extreme stresses of the GaN epi process.
- Okmetic technology was developed in close co-operation with several industrial players utilizing all the widely used GaN production processes.
- Customized wafers simplify the epitaxial process setup, tuning and ramping-up to production.
- Full wafer shape analysis is available as part of the wafer tailoring.

WIDE SELECTION OF WAFER PARAMETERS TO MATCH YOUR APPLICATION NEEDS

- Custom wafer thickness options to reduce wafer bow and warpage (150- 200 mm up to 1,150 µm).
- LTO option for the back surface for further stress management.
- Up to > 10,000 Ohm-cm resistivity with suitable Oi control, balancing between resistivity stability and lattice integrity.
- Option for high resistivity on-orientation <111> with tight orientation control.
- Option for GaN-on-SOI substrates e.g. for new HEMT devices (High-Electron-Mobility Transistor).



SUPERIOR PERFORMANCE

Okmetic GaN-on-Si optimized wafers have consistently shown superior performance in GaN-on-Si epitaxy. During the GaN epi process, wafer curvature is monitored and controlled. Okmetic wafer bow returns close to the initial stage after GaN stack deposition process. This is illustrated on the left in the gematrical mapping of Okmetic Si substrate processed into a GaN-on-Si wafer at Aalto University.